**Unit 1**

1. Show the general structure of IAS Computer & Explain
2. Draw Flowchart of Booth Algorithm.
3. Draw flowchart of Non-Restoring Division algorithm.
4. Draw flowchart for Restoring division algorithm.
5. With a neat diagram, describe the functional units of a computer. Give few examples for I/O devices.
6. Discuss IEEE standard for single precision and double precision floating point numbers, with standard notations.
7. Perform Binary signed multiplication on the following pair of Numbers -7 and +3.
8. Perform Binary unsigned multiplication on the following pair of Numbers 5 and 4.
9. Perform subtraction on the following pairs of numbers using 5-bit signed 2’s complement format. Indicate about overflow in each case:

a)+10 and -8 b) +12 and +9 c)-15 and -9 d) -14 and +5

1. Explain the bus structure
2. Represent 85.125 in IEEE floating point using single precision and double precision.
3. Explain the three bus organisation of processor and its advantages.

**Unit 2:**

1. Draw a Pin-Out structure for 8086 processor.
2. Draw architecture for 8086 processor and explain very component in detail.
3. Explain following with an example

* Direct addressing mode
* Index addressing mode
* Register addressing mode

1. What is addressing mode? Explain any five type of addressing mode with an example.
2. Compare the CISC and RISC

**Unit 3:**

1. With the block diagram, describe the organisation of hardwired control unit
2. Explain Single bus organisation
3. Differentiate hardwired control unit over the Micro-programmed Control.
4. Write a control sequence for the following instruction for single bus organisation

SUB (R3), R1

1. Write a control sequence for the following instruction for single bus organisation

MOVE (R1), R2.

1. Describe the sequence of control signals to be generated to fetch an instruction from memory in a single bus organisation.

**Unit 4**

1. IIiustrate memory hierarchy with diagram.
2. Briefly explain any four ROM types.
3. Discuss dynamic memory cell.
4. Write note on Virtual memory.
5. With figure, explain Internal organisation of 4M x 4 dynamic memory chip.
6. IIiustrate Internal structure of static memory.
7. What is cache memory? Explain direct mapping technique with diagram?
8. What is mapping function? Explain set associative mapping techniques with diagram.
9. What are the various hazards in instruction pipelining? Explain?
10. What is pipelining? Explain Branch hazard in detail?
11. Explain Loop buffer?
12. Explain branch prediction with state diagram?
13. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-

* Number of bits in tag
* Tag directory size

1. Consider 2 way set associative map cache of size 16kb with block size 256 bytes the size of main memory is 128 kb find-

* Number of bits in tag
* Tag directory size

**Unit 5**

What is parallel processing? Explain Flynn’s classification in detail.

Write a note on handles classification

Explain message passing in parallel processing.

Explain Tightly coupled multiprocessor with block diagram.

Calculate maximum speed up in the performance, If 90% of a calculation is parallelized with 10 processors using amdahl’s law.

**Unit 6**

List the basic difference between CPU and GPU architecture.

What are the three general section of CUDA program.

Explain Kernel, Thread and Block with reference to GPU.

Explain architecture of Modern GPU with block diagram.